

TB-6V-LX240T/365T/550T/SX475T-PCIEXP Hardware User's Manual

Rev.1.03

Revision History

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1. Introduction

Thank you for purchasing the TB-6V-LX240/365T/550T/SX475T-PCIEXP board.

Before using the product, be sure to carefully read this User Manual and fully understand how to correctly use the product.

Read through this manual and always keep it handy.




Safety Precautions

Be sure to observe these precautions




Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**












The following conventions are used to indicate and classify precautions in this manual. Failure to observe precautions can result in injury to people or damage to property.



 Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
 Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
 Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Be sure to turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

**Warning**

	
	<p>In the event of a failure, disconnect the power supply.</p> <p>If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.</p>
	<p>If an unpleasant smell or smoking occurs, disconnect the power supply.</p> <p>If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that no smoking is observed, contact our sales personnel for repair.</p>
	<p>Do not disassemble, repair or modify the product.</p> <p>Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.</p>
	<p>Do not touch a cooling fan (when installing it).</p> <p>As a cooling fan rotates in high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.</p>
	<p>Do not place the product on unstable locations.</p> <p>Otherwise, it may drop or fall, resulting in injury to persons or failure.</p>
	<p>If the product is dropped or damaged, do not use it as is.</p> <p>Otherwise, a fire or electric shock may occur.</p>
	<p>Do not touch the product with a metallic object.</p> <p>Otherwise, a fire or electric shock may occur.</p>
	<p>Do not place the product in dusty or humid locations or where water may splash.</p> <p>Otherwise, a fire or electric shock may occur.</p>
	<p>Do not get the product wet or touch it with a wet hand.</p> <p>Otherwise, the product may break down or it may cause a fire, smoking or electric shock.</p>
	<p>Do not touch a connector (gold-plated portion) on the product.</p> <p>Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.</p>

 Caution	
	Do not use or place the product in the following locations. <ul style="list-style-type: none"> • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Staticky locations • Locations close to water or chemicals <p>Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.</p>
	Do not place heavy things on the product. <p>Otherwise, the product may be damaged.</p>

Disclaimer

This product is the Xilinx Virtex6 FPGA evaluation board. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

- Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse or use under other abnormal conditions,
- Secondary impact arising from use of this product or its unusable state (business interruption or others),
- Use of this product against the instructions given in this manual or
- Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

- Erasure or corruption of data arising from use of this product
- Any consequences or other abnormalities arising from use of this product, or
- Damage of this product not due to our responsibility or failure due to modification

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.

Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.

The specification of this product is subject to change without prior notice.

The product is subject to discontinuation without prior notice.

- Be careful when inserting a memory module into the onboard DIMM socket.
(Limit the number of trials of inserting the memory module into the DIMM socket to 25)

2. Related Documents and Board Accessories

Related documents:

All documents relating to this board can be downloaded from our website. Please refer to attached paper of the products.

Board Fixer:

- Fan/heat sink set
Fan: 1 Heat sink: 1 M3 X 20 screw: 2 Washer: 2
XH connector (JST: B3B-XH-A): 1
- DDR3-SO-DIMM
1G byte: (SanMax SMD-N1G88-13H or equivalent): 2

Board Accessories:

- Board foot set
Rubber foot: 7 M3 X 6 screw: 14 M3 X 10 spacer: 7
- AC/DC power supply
12V/15A power supply: 1
- AC power supply cable with a power switch: 1
- DC power supply cable: 1
- microSD card for Config:
2Gbyte: 1

3. Overview

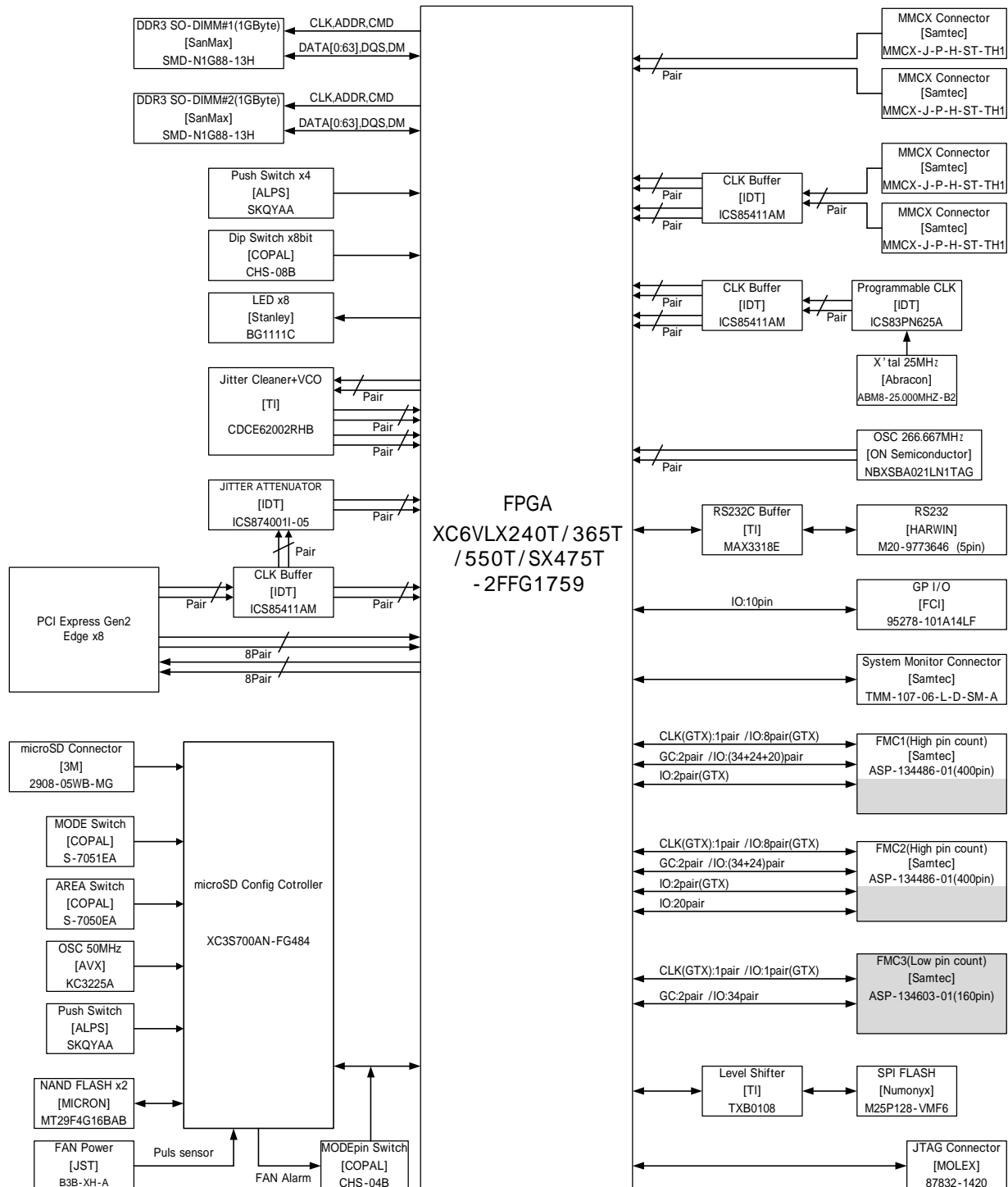
This board is the high-speed and high-density **PCI Express Gen2** evaluation board equipped with Xilinx Virtex6 Series FPGA "XC6VLX240T/365T/550T-2FFG1759" or "XC6VSX475T-2FFG1759".

4. Feature

- PCI Express Gen2(x8) interface
- High-Pin Count FMC connector x 2 and Low-Pin Count FMC connector x 1
Due to limitation of the number of FPGA pins, all the defined FMC connector pins are not connected.
For more information, refer to the corresponding connector pinout table contained in this document.
- DDR3 SO-DIMM 1GB x 2: **SanMax SMD-N1G88-13H (1GByte x 2) 1066Mbps**
- Various clock sources
- For setting: PushSWs DipSWs PinHeaders
- For monitoring: LEDs
- Configuration via microSD Card
- NAND Memory for CONFIG to support high-speed configuration x 2

5. Block Diagram

The following figure shows the block diagram of this board.



Note: The gray areas are supported by the TB-6VLX550T/SX475T-PCIEXP.

Figure5-1 Block Diagram

6. External View of the Board

The following figures show the external views of the board.

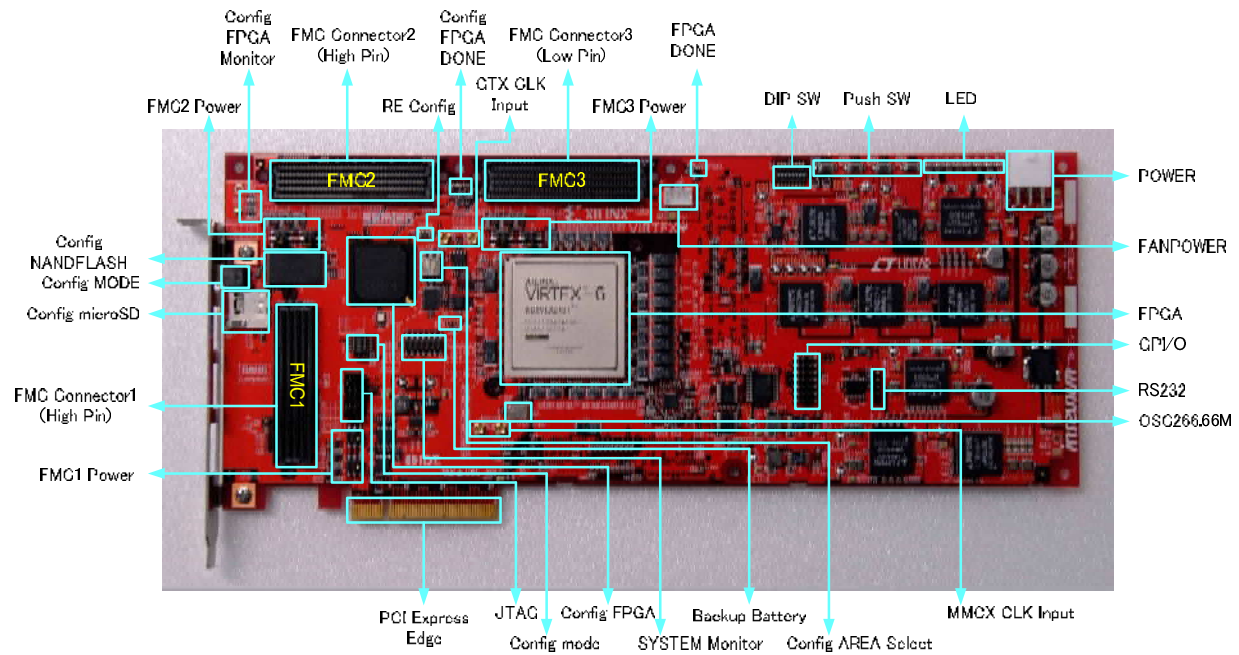


Figure6-1 Component Side of the Board

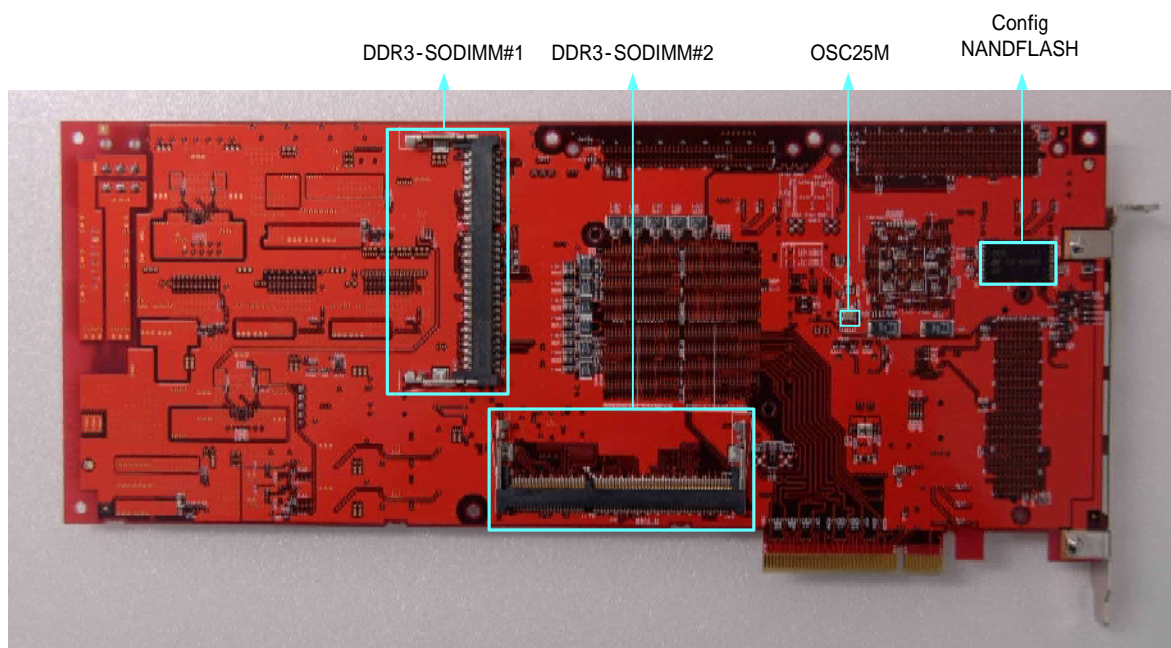


Figure6-2 Solder Side of the Board

7. Board Specification

External Dimensions:	W:300mm x H:130mm (non-compliance with PCI-Express specification)
Number of Layers:	16 Layers
Board Thickness:	1.7mm
Material:	FR-4
FPGA	Xilinx XC6VLX240T/365T/550T-2FFG1759 / XC6VSX475T-2FFG1759
SPI-FLASH:	Numonyx M25P128-VMF6
FMC Connector (High-Pin):	Samtec ASP-134486-01
FMC Connector (Low-Pin):	Samtec ASP-134603-01
DDR3 SO-DIMM:	SanMax SMD-N1G88-13H
MMCX Connector:	Samtec MMCX-J-P-H-ST-TH1
General-Purpose I/F(GPIO):	FCI 95278-101A14LF

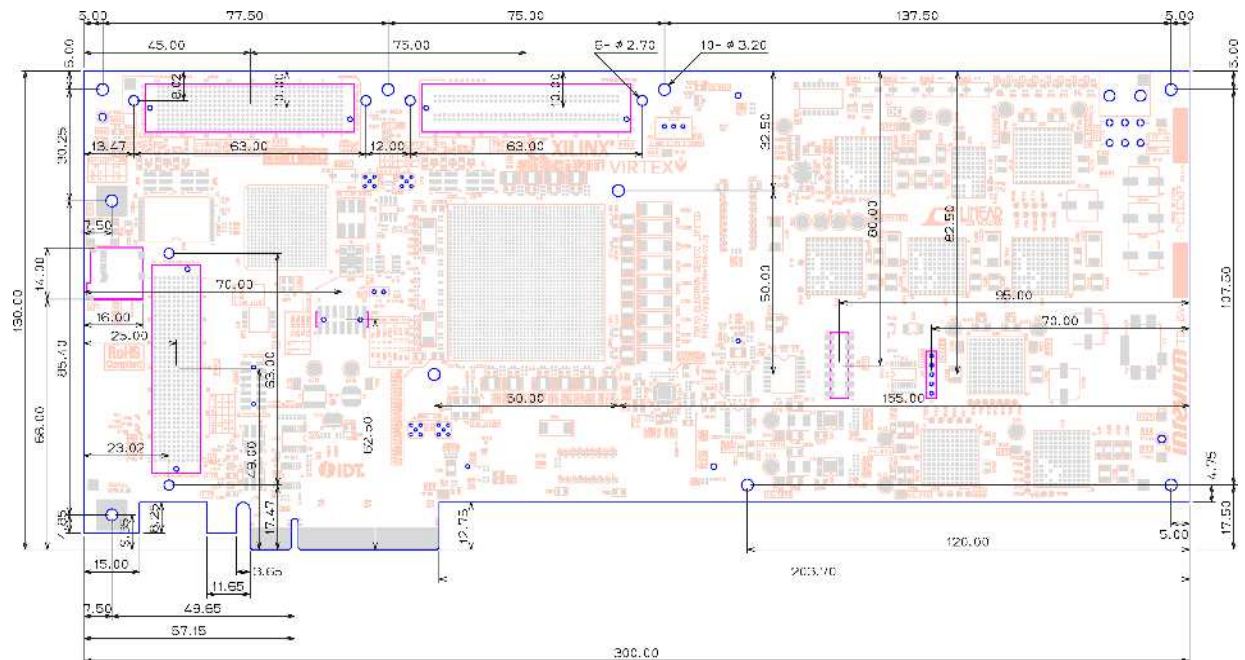


Figure7-1 Board Dimension Diagram

8. Description of Each Component

8.1. Power Supply Structure

The following figure provides the internal power supply structure.

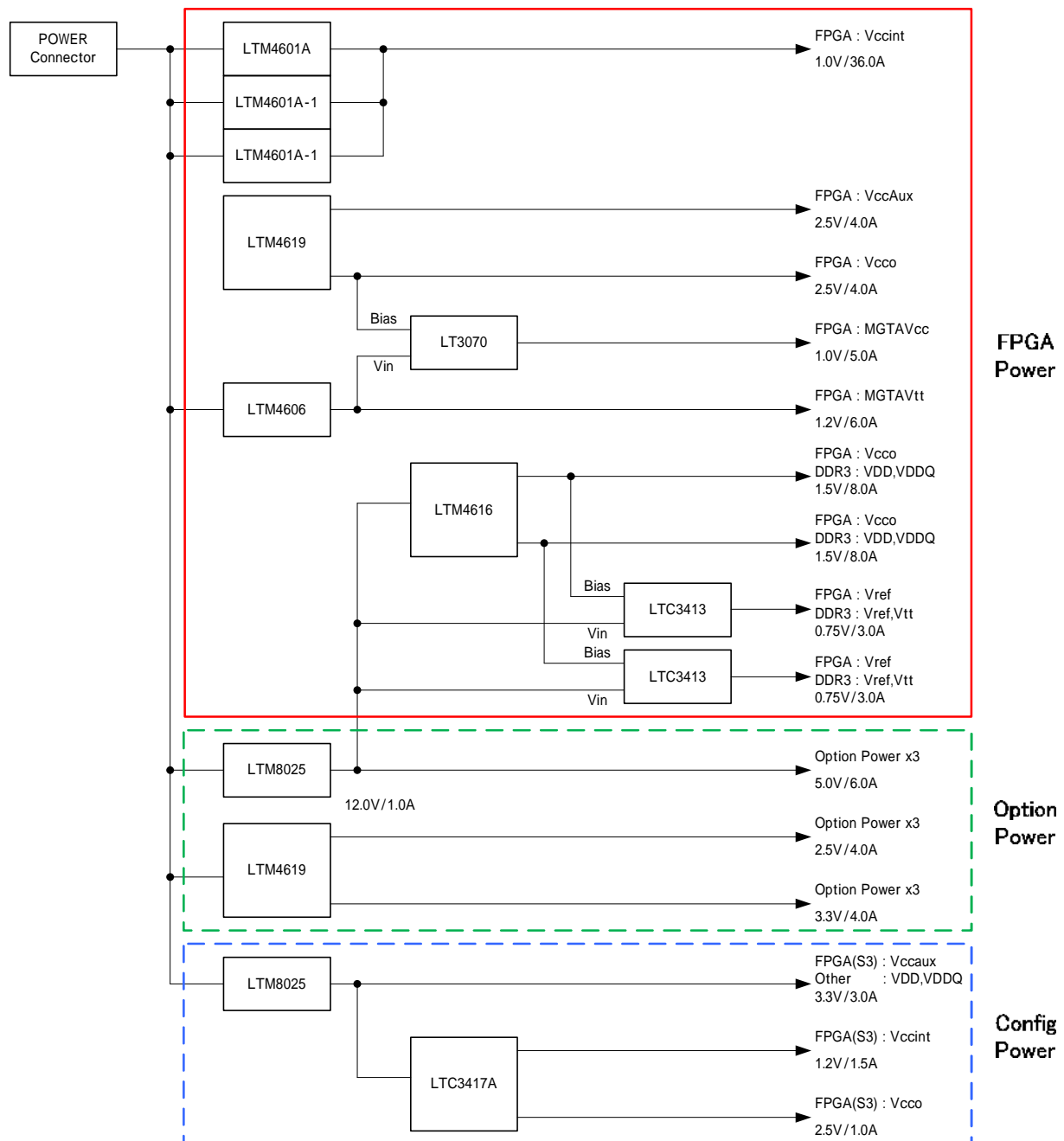


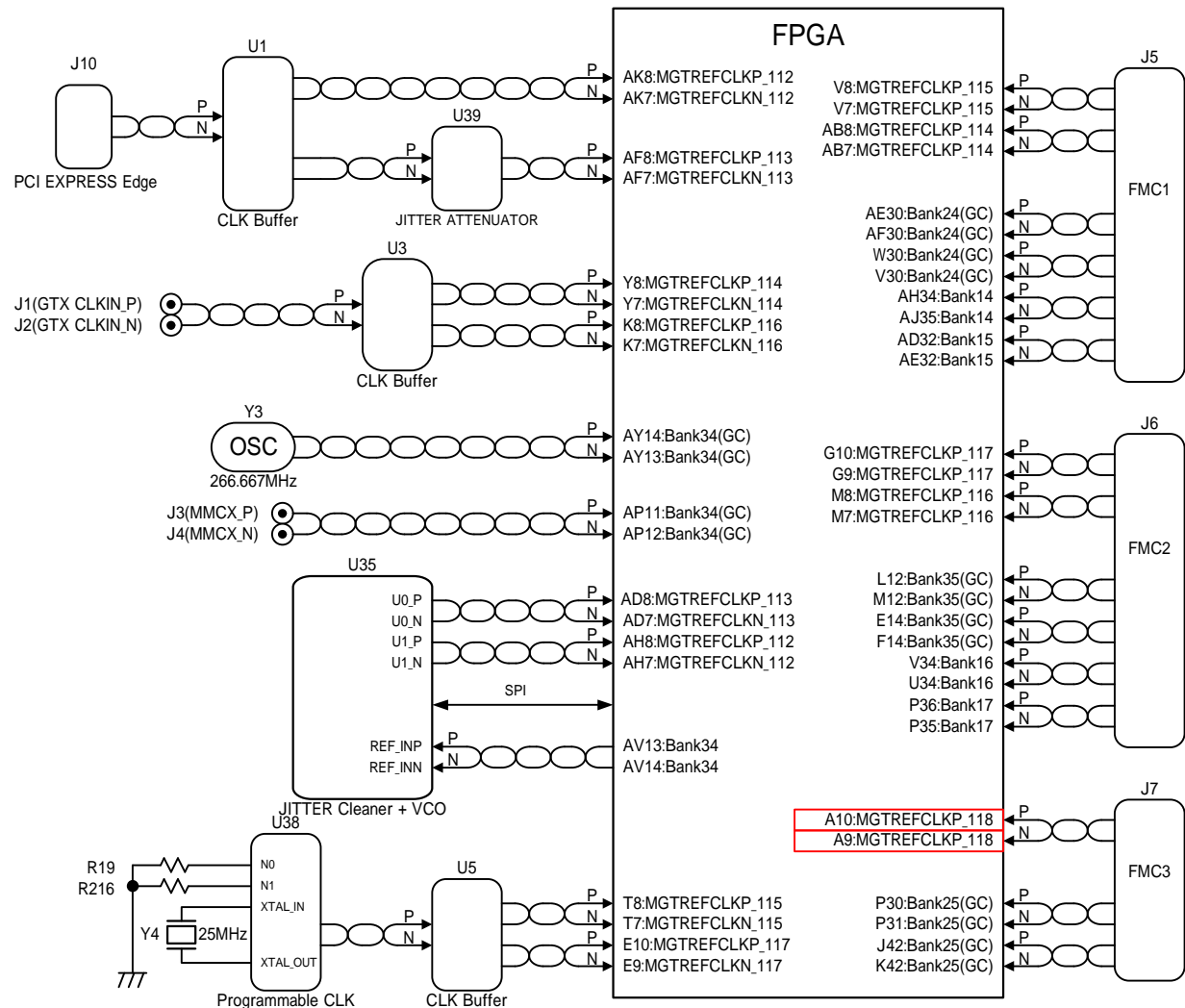
Figure8-1 Power Supply Structure

About power supply input:

The power is provided through a 12V ATX power connector.

8.2. Oscillator

This board provides the following clock sources.



Note: The portion in redline box is supported by TB-6VLX550T/SX475T-PCIEXP.

Figure8-2 Clock Structure

Table 1 Details of Onboard Oscillator

Connection	Name	I/F	PIN	Remarks
J10	PCIe_100M_MGT_P/N PCIe_250M_MGT_P/N	LVDS	AK8/AK7 AF8/AF7	PIC Express Edge > via Difference Buffer Difference Buffer > via Jitter Attenuator
J1/J2	GTX_CLK1_P/N GTX_CLK2_P/N	LVDS	Y8/Y7 K8/K7	MGT reference external clock
Y3	CLK266M_P/N	LVDS	AY14/AY13	DDR3 (IDelay) clock
J3/J4	MMCX_CLK_P/N	LVDS	AP11/AP12	MMCX external clock
FPGA (AV13/AV14pin)	JC_CLK0_P/N JC_CLK1_P/N	LVDS	AD8/AD7 AH8/AH7	MGT Reference Clock FPGA(AV13/AV14): FPGA output clock Jitter cleaner
Y4	GTX_312M_1_P/N GTX_312M_2_P/N	LVDS	T8/T7 E10/E9	MGT Reference Clock Clock Generator > via Difference Buffer
FMC1(J5)	FMC1_GBTCLK0_M2C_P/N	LVDS	AB8/AB7	FMC1 Gigabit data clock
FMC1(J5)	FMC1_GBTCLK1_M2C_P/N	LVDS	V8/V7	FMC1 Gigabit data clock
FMC1(J5)	FMC1_CLK0_M2C_P/N	LVDS	AE30/AF30	FMC1 Reference Clock
FMC1(J5)	FMC1_CLK1_M2C_P/N	LVDS	W30/V30	FMC1 Reference Clock
FMC1(J5)	FMC1_CLK2_M2C_P/N	LVDS	AH34/AJ35	FMC1 Reference Clock
FMC1(J5)	FMC1_CLK3_M2C_P/N	LVDS	AD32/AE32	FMC1 Reference Clock
FMC2(J6)	FMC2_GBTCLK0_M2C_P/N	LVDS	M8/M7	FMC2 Gigabit data clock
FMC2(J6)	FMC2_GBTCLK1_M2C_P/N	LVDS	G10/G9	FMC2 Gigabit data clock
FMC2(J6)	FMC2_CLK0_M2C_P/N	LVDS	L12/M12	FMC2 Reference Clock
FMC2(J6)	FMC2_CLK1_M2C_P/N	LVDS	E14/F14	FMC2 Reference Clock
FMC2(J6)	FMC2_CLK2_M2C_P/N	LVDS	V34/U34	FMC2 Reference Clock
FMC2(J6)	FMC2_CLK3_M2C_P/N	LVDS	P36/P35	FMC2 Reference Clock
FMC3(J7)	FMC3_GBTCLK0_M2C_P/N	LVDS	A10/A9	FMC2 Gigabit data clock
FMC3(J7)	FMC3_CLK0_M2C_P/N	LVDS	P30/P31	FMC2 Reference Clock
FMC3(J7)	FMC3_CLK1_M2C_P/N	LVDS	J42/K42	FMC2 Reference Clock

FMC*_CLK*_M2C_P/N does not need to be LVDS (differential).

8.3. FMC Connector Interface

This board has three Samtec FMC connectors.

High-Pin Count: 2 (J5,6)

Low-Pin Count: 1 (J7)

The following provides the pinout table. **Note that all HPC and LPC pins are not connected to the FPGA.**

	K	J	H	G	F	E	D	C	B	A
1	VREF B M2C	GND	VREF A M2C	GND	PG M2C	GND	PG C2M	GND	RES1	GND
2	GND	CLK3 M2C P	PRSN1 M2C L	CLK1 M2C P	GND	HA01 P CC	GND	DP0 C2M P	GND	DP1 M2C P
3	GND	CLK3 M2C N	GND	CLK1 M2C N	GND	HA01 N CC	GND	DP0 C2M N	GND	DP1 M2C N
4	CLK2 M2C P	GND	CLK0 M2C P	GND	HA00 P CC	GND	GBTCLK0 M2C P	GND	DP9 M2C P	GND
5	CLK2 M2C N	GND	CLK0 M2C N	GND	HA00 N CC	GND	GBTCLK0 M2C N	GND	DP9 M2C N	GND
6	GND	HA03 P	GND	LA00 P CC	GND	HA05 P	GND	DP0 M2C P	GND	DP2 M2C P
7	HA02 P	HA03 N	LA02 P	LA00 N CC	HA04 P	HA05 N	GND	DP0 M2C N	GND	DP2 M2C N
8	HA02 N	GND	LA02 N	GND	HA04 N	GND	LA01 P CC	GND	DP8 M2C P	GND
9	GND	HA07 P	GND	LA03 P	GND	HA09 P	LA01 N CC	GND	DP8 M2C N	GND
10	HA06 P	HA07 N	LA04 P	LA03 N	HA08 P	HA09 N	GND	LA06 P	GND	DP3 M2C P
11	HA06 N	GND	LA04 N	GND	HA08 N	GND	LA05 P	LA06 N	GND	DP3 M2C N
12	GND	HA11 P	GND	LA08 P	GND	HA13 P	LA05 N	GND	DP7 M2C P	GND
13	HA10 P	HA11 N	LA07 P	LA08 N	HA12 P	HA13 N	GND	GND	DP7 M2C N	GND
14	HA10 N	GND	LA07 N	GND	HA12 N	GND	LA09 P	LA10 P	GND	DP4 M2C P
15	GND	HA14 P	GND	LA12 P	GND	HA16 P	LA09 N	LA10 N	GND	DP4 M2C N
16	HA17 P CC	HA14 N	LA11 P	LA12 N	HA15 P	HA16 N	GND	GND	DP6 M2C P	GND
17	HA17 N CC	GND	LA11 N	GND	HA15 N	GND	LA13 P	GND	DP6 M2C N	GND
18	GND	HA18 P	GND	LA16 P	GND	HA20 P	LA13 N	LA14 P	GND	DP5 M2C P
19	HA21 P	HA18 N	LA15 P	LA16 N	HA19 P	HA20 N	GND	LA14 N	GND	DP5 M2C N
20	HA21 N	GND	LA15 N	GND	HA19 N	GND	LA17 P CC	GND	GBTCLK1 M2C P	GND
21	GND	HA22 P	GND	LA20 P	GND	HB03 P	LA17 N CC	GND	GBTCLK1 M2C N	GND
22	HA23 P	HA22 N	LA19 P	LA20 N	HB02 P	HB03 N	GND	LA18 P CC	GND	DP1 C2M P
23	HA23 N	GND	LA19 N	GND	HB02 N	GND	LA23 P	LA18 N CC	GND	DP1 C2M N
24	GND	HB01 P	GND	LA22 P	GND	HB05 P	LA23 N	GND	DP9 C2M P	GND
25	HB00 P CC	HB01 N	LA21 P	LA22 N	HB04 P	HB05 N	GND	GND	DP9 C2M N	GND
26	HB00 N CC	GND	LA21 N	GND	HB04 N	GND	LA26 P	LA27 P	GND	DP2 C2M P
27	GND	HB07 P	GND	LA25 P	GND	HB09 P	LA26 N	LA27 N	GND	DP2 C2M N
28	HB06 P CC	HB07 N	LA24 P	LA25 N	HB08 P	HB09 N	GND	GND	DP8 C2M P	GND
29	HB06 N CC	GND	LA24 N	GND	HB08 N	GND	TCK	GND	DP8 C2M N	GND
30	GND	HB11 P	GND	LA29 P	GND	HB13 P	TDI	SCL	GND	DP3 C2M P
31	HB10 P	HB11 N	LA28 P	LA29 N	HB12 P	HB13 N	TDO	SDA	GND	DP3 C2M N
32	HB10 N	GND	LA28 N	GND	HB12 N	GND	3P3VAUX	GND	DP7 C2M P	GND
33	GND	HB15 P	GND	LA31 P	GND	HB19 P	TMS	GND	DP7 C2M N	GND
34	HB14 P	HB15 N	LA30 P	LA31 N	HB16 P	HB19 N	TRST L	GA0	GND	DP4 C2M P
35	HB14 N	GND	LA30 N	GND	HB16 N	GND	GA1	12P0V	GND	DP4 C2M N
36	GND	HB18 P	GND	LA33 P	GND	HB21 P	3P3V	GND	DP6 C2M P	GND
37	HB17 P CC	HB18 N	LA32 P	LA33 N	HB20 P	HB21 N	GND	12P0V	DP6 C2M N	GND
38	HB17 N CC	GND	LA32 N	GND	HB20 N	GND	3P3V	GND	GND	DP5 C2M P
39	GND	VIO B M2C	GND	VAD0	GND	VAD0	GND	3P3V	GND	DP5 C2M N
40	VIO B M2C	GND	VAD0	GND	VAD0	GND	3P3V	GND	RES0	GND

LPC Connector

LPC Connector

LPC Connector

LPC Connector

Figure8-3 High-Pin Cont Pin Layout

	K	J	H	G	F	E	D	C	B	A
1	NC	NC	VREF A M2C	GND	NC	NC	PG C2M	GND	NC	NC
2	NC	NC	PRSN1 M2C L	CLK1 M2C P	NC	NC	GND	DP0 C2M P	NC	NC
3	NC	NC	GND	CLK1 M2C N	NC	NC	GND	DP0 C2M N	NC	NC
4	NC	NC	CLK0 M2C P	GND	NC	NC	GBTCLK0 M2C P	GND	NC	NC
5	NC	NC	CLK0 M2C N	GND	NC	NC	GBTCLK0 M2C N	GND	NC	NC
6	NC	NC	GND	LA00 P CC	NC	NC	GND	DP0 M2C P	NC	NC
7	NC	NC	LA02 P	LA00 N CC	NC	NC	GND	DP0 M2C N	NC	NC
8	NC	NC	LA02 N	GND	NC	NC	LA01 P CC	GND	NC	NC
9	NC	NC	GND	LA03 P	NC	NC	LA01 N CC	GND	NC	NC
10	NC	NC	LA04 P	LA03 N	NC	NC	GND	LA06 P	NC	NC
11	NC	NC	LA04 N	LA03 N	NC	NC	LA05 P	LA06 N	NC	NC
12	NC	NC	GND	LA08 P	NC	NC	LA05 N	GND	NC	NC
13	NC	NC	LA07 P	LA08 N	NC	NC	GND	GND	NC	NC
14	NC	NC	LA07 N	GND	NC	NC	LA09 P	LA10 P	NC	NC
15	NC	NC	GND	LA12 P	NC	NC	LA09 N	LA10 N	NC	NC
16	NC	NC	LA11 P	LA12 N	NC	NC	GND	GND	NC	NC
17	NC	NC	LA11 N	GND	NC	NC	LA13 P	GND	NC	NC
18	NC	NC	GND	LA16 P	NC	NC	LA13 N	LA14 P	NC	NC
19	NC	NC	LA15 P	LA16 N	NC	NC	GND	LA14 N	NC	NC
20	NC	NC	LA15 N	GND	NC	NC	LA17 P CC	GND	NC	NC
21	NC	NC	GND	LA20 P	NC	NC	LA17 N CC	GND	NC	NC
22	NC	NC	LA19 P	LA20 N	NC	NC	GND	LA18 P CC	NC	NC
23	NC	NC	LA19 N	GND	NC	NC	LA23 P	LA18 N CC	NC	NC
24	NC	NC	GND	LA22 P	NC	NC	LA23 N	GND	NC	NC
25	NC	NC	LA21 P	LA22 N	NC	NC	GND	GND	NC	NC
26	NC	NC	LA21 N	GND	NC	NC	LA26 P	LA27 P	NC	NC
27	NC	NC	GND	LA25 P	NC	NC	LA26 N	LA27 N	NC	NC
28	NC	NC	LA24 P	LA25 N	NC	NC	GND	GND	NC	NC
29	NC	NC	LA24 N	GND	NC	NC	TCK	GND	NC	NC
30	NC	NC	GND	LA29 P	NC	NC	TDI	SCL	NC	NC
31	NC	NC	LA28 P	LA29 N	NC	NC	TDO	SDA	NC	NC
32	NC	NC	LA28 N	GND	NC	NC	3P3VAUX	GND	NC	NC
33	NC	NC	GND	LA31 P	NC	NC	TMS	GND	NC	NC
34	NC	NC	LA30 P	LA31 N	NC	NC	TRST L	GA0	NC	NC
35	NC	NC	LA30 N	GND	NC	NC	GA1	12P0V	NC	NC
36	NC	NC	GND	LA33 P	NC	NC	3P3V	GND	NC	NC
37	NC	NC	LA32 P	LA33 N	NC	NC	GND	12P0V	NC	NC
38	NC	NC	LA32 N	GND	NC	NC	3P3V	GND	NC	NC
39	NC	NC	GND	VAD0	NC	NC	GND	3P3V	NC	NC
40	NC	NC	VAD0	GND	NC	NC	3P3V	GND	NC	NC

LPC Connector

LPC Connector

LPC Connector

LPC Connector

Figure8-4 Low-Pin Cont Pin Layout

8.3.1. FMC1 HPC Connector (High-Pin Count)

The board uses the High-Pin Count connector. Due to limitation of the number of FPGA pins (Banks), all FMC connector pins are not connected. The connector is interfaced as shown below.

HighSpeed: XC6VLX240T/365T TX 8ch RX 8ch
 XC6VLX550T/XC6VSX475T TX 10ch RX 10ch
 LowSpeed: XC6VLX240T/365T LA 34Pair (72) HA 24Pair (48) HB 20Pair (40)
 XC6VLX550T/XC6VSX475T LA 34Pair (72) HA 24Pair (48) HB 20Pair (40)

Table 2 shows the FMC1 HPC connector pinout table for FPGA.

Table 2 FMC1 Connector Pinout

Bank No.	Pin No.	A		B	PinNo.	Bank No.
		GND	1	*1 RES1	TP80	
MGTRXP3_115	R5	DP1_M2C_P	2	GND		
MGTRXN3_115	R6	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	AU5	MGTRXP1_111
		GND	5	DP9_M2C_N	AU6	MGTRXN1_111
MGTRXP1_115	V3	DP2_M2C_P	6	GND		
MGTRXN1_115	V4	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	AV7	MGTRXP0_111
		GND	9	DP8_M2C_N	AV8	MGTRXN0_111
MGTRXP0_115	W5	DP3_M2C_P	10	GND		
MGTRXN0_115	W6	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	Y3	MGTRXP3_114
		GND	13	DP7_M2C_N	Y4	MGTRXN3_114
MGTRXP2_114	AA5	DP4_M2C_P	14	GND		
MGTRXN2_114	AA6	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	AB3	MGTRXP1_114
		GND	17	DP6_M2C_N	AB4	MGTRXN1_114
MGTRXP0_114	AC5	DP5_M2C_P	18	GND		
MGTRXN0_114	AC6	DP5_M2C_N	19	GND		
		GND	20	GBTCLK1_M2C_P	AB8	MGTREFCLK0P_114
		GND	21	GBTCLK1_M2C_N	AB7	MGTREFCLK0N_114
MGTTXP3_115	P3	DP1_C2M_P	22	GND		
MGTTXN3_115	P4	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	AU1	MGTTXP1_111
		GND	25	DP9_C2M_N	AU2	MGTTXN1_111
MGTTXP1_115	T3	DP2_C2M_P	26	GND		
MGTTXN1_115	T4	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	AV3	MGTTXP0_111
		GND	29	DP8_C2M_N	AV4	MGTTXN0_111
MGTTXP0_115	U1	DP3_C2M_P	30	GND		
MGTTXN0_115	U2	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	W1	MGTTXP3_114
		GND	33	DP7_C2M_N	W2	MGTTXN3_114
MGTTXP2_114	AA1	DP4_C2M_P	34	GND		
MGTTXN2_114	AA2	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	AC1	MGTTXP1_114
		GND	37	DP6_C2M_N	AC2	MGTTXN1_114
MGTTXP0_114	AE1	DP5_C2M_P	38	GND		
MGTTXN0_114	AE2	DP5_C2M_N	39	GND		
		GND	40	*1 RES0	TP89	

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	*5 PG_C2M		
MGTTXP2_115	R1	DP0_C2M_P	2	GND		
MGTTXN2_115	R2	DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P	V8	MGTREFCLK0P_115
		GND	5	GBTCLK0_M2C_N	V7	MGTREFCLK0N_115
MGTRXP2_115	U5	DP0_M2C_P	6	GND		
MGTRXN2_115	U6	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	AV41	13
		GND	9	LA01_N_CC	AU41	13
13	AR39	LA06_P	10	GND		
13	AT39	LA06_N	11	LA05_P	AV40	13
		GND	12	LA05_N	AW40	13
		GND	13	GND		
13	BA41	LA10_P	14	LA09_P	BA40	13
13	BB41	LA10_N	15	LA09_N	AY40	13
		GND	16	GND		
		GND	17	LA13_P	AN39	13
13	AP42	LA14_P	18	LA13_N	AM39	13
13	AR42	LA14_N	19	GND		
		GND	20	LA17_P_CC	AC36	15
		GND	21	LA17_N_CC	AB36	15
15	AC41	LA18_P_CC	22	GND		
15	AD41	LA18_N_CC	23	LA23_P	AE40	15
		GND	24	LA23_N	AE39	15
		GND	25	GND		
15	AC40	LA27_P	26	LA26_P	AD42	15
15	AD40	LA27_N	27	LA26_N	AE42	15
		GND	28	GND		
		GND	29	*4 TCK		
		*2 SCL	30	*4 TDI		
		*2 SDA	31	*4 TDO		
		GND	32	3P3VAUX		
		GND	33	*4 TMS		
		*3 GA0	34	*4 TRST_L		
		12P0V	35	*3 GA1		
		GND	36	3P3V		
		12P0V	37	GND		
		GND	38	3P3V		
		3P3V	39	GND		
		GND	40	3P3V		

Bank No.	Pin No.	E		F	PinNo.	Bank No.
		GND	1	*5 PG_M2C		
14	AH39	HA01_P_CC	2	GND		
14	AJ40	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	AK38	14
		GND	5	HA00_N_CC	AJ38	14
14	AF32	HA05_P	6	GND		
14	AG33	HA05_N	7	HA04_P	AG34	14
		GND	8	HA04_N	AF34	14
14	AF35	HA09_P	9	GND		
14	AF36	HA09_N	10	HA08_P	AG36	14
		GND	11	HA08_N	AH36	14
14	AF37	HA13_P	12	GND		
14	AG37	HA13_N	13	HA12_P	AG38	14
		GND	14	HA12_N	AH38	14
14	AK39	HA16_P	15	GND		
14	AL39	HA16_N	16	HA15_P	AK40	14
		GND	17	HA15_N	AL40	14
35	H14	HA20_P	18	GND		
35	G13	HA20_N	19	HA19_P	F12	35
		GND	20	HA19_N	E12	35
12	AU36	HB03_P	21	GND		
12	AT36	HB03_N	22	HB02_P	AR35	12
		GND	23	HB02_N	AT35	12
12	AV34	HB05_P	24	GND		
12	AV35	HB05_N	25	HB04_P	AW36	12
		GND	26	HB04_N	AV36	12
12	BB34	HB09_P	27	GND		
12	BA34	HB09_N	28	HB08_P	BA35	12
		GND	29	HB08_N	AY35	12
12	BA37	HB13_P	30	GND		
12	BB37	HB13_N	31	HB12_P	AY38	12
		GND	32	HB12_N	AY37	12
12	AY39	HB19_P	33	GND		
12	BA39	HB19_N	34	HB16_P	AV39	12
		GND	35	HB16_N	AV38	12
		HB21_P	36	GND		
		HB21_N	37	HB20_P		
		GND	38	HB20_N		
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*7 VREF_A_M2C		
24	W30	CLK1_M2C_P	2	*6 PRSNT_M2C_L	AT40	13
24	V30	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	AE30	24
		GND	5	CLK0_M2C_N	AF30	24
13	AR40	LA00_P_CC	6	GND		
13	AT41	LA00_N_CC	7	LA02_P	AN41	13
		GND	8	LA02_N	AP41	13
13	AK35	LA03_P	9	GND		
13	AL36	LA03_N	10	LA04_P	AL37	13
		GND	11	LA04_N	AM38	13
13	AN40	LA08_P	12	GND		
13	AP40	LA08_N	13	LA07_P	AW42	13
		GND	14	LA07_N	AW41	13
13	AY42	LA12_P	15	GND		
13	BA42	LA12_N	16	LA11_P	AT42	13
		GND	17	LA11_N	AU42	13
13	AM37	LA16_P	18	GND		
13	AM36	LA16_N	19	LA15_P	AM34	13
		GND	20	LA15_N	AL35	13
15	AE34	LA20_P	21	GND		
15	AE35	LA20_N	22	LA19_P	AE38	15
		GND	23	LA19_N	AD38	15
15	AF42	LA22_P	24	GND		
15	AF41	LA22_N	25	LA21_P	AD36	15
		GND	26	LA21_N	AD35	15
15	AA42	LA25_P	27	GND		
15	AB42	LA25_N	28	LA24_P	AA41	15
		GND	29	LA24_N	AB41	15
15	AC35	LA29_P	30	GND		
15	AB34	LA29_N	31	LA28_P	AB39	15
		GND	32	LA28_N	AA40	15
15	AC34	LA31_P	33	GND		
15	AC33	LA31_N	34	LA30_P	AC38	15
		GND	35	LA30_N	AC39	15
15	AE33	LA33_P	36	GND		
15	AD33	LA33_N	37	LA32_P	AB37	15
		GND	38	LA32_N	AB38	15
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	J		K	PinNo.	Bank No.
		GND	1	*7 VREF_B_M2C		
15	AD32	CLK3_M2C_P	2	GND		
15	AE32	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	AH34	14
		GND	5	CLK2_M2C_N	AJ35	14
14	AF39	HA03_P	6	GND		
14	AG39	HA03_N	7	HA02_P	AF40	14
		GND	8	HA02_N	AG41	14
14	AG42	HA07_P	9	GND		
14	AH41	HA07_N	10	HA06_P	AH40	14
		GND	11	HA06_N	AJ41	14
14	AJ42	HA11_P	12	GND		
14	AK42	HA11_N	13	HA10_P	AL42	14
		GND	14	HA10_N	AM42	14
14	AL41	HA14_P	15	GND		
14	AM41	HA14_N	16	HA17_P_CC	J12	35
		GND	17	HA17_N_CC	J11	35
35	M14	HA18_P	18	GND		
35	N14	HA18_N	19	HA21_P	H15	35
		GND	20	HA21_N	G14	35
35	D16	HA22_P	21	GND		
35	C16	HA22_N	22	HA23_P	A16	35
		GND	23	HA23_N	B16	35
12	AU34	HB01_P	24	GND		
12	AT34	HB01_N	25	HB00_P_CC	AP36	12
		GND	26	HB00_N_CC	AP35	12
12	AY34	HB07_P	27	GND		
12	AW35	HB07_N	28	HB06_P_CC	AN35	12
		GND	29	HB06_N_CC	AN36	12
12	BB36	HB11_P	30	GND		
12	BA36	HB11_N	31	HB10_P	BB39	12
		GND	32	HB10_N	BB38	12
12	AU37	HB15_P	33	GND		
12	AU38	HB15_N	34	HB14_P	AT37	12
		GND	35	HB14_N	AR38	12
12	AP37	HB18_P	36	GND		
12	AR37	HB18_N	37	HB17_P_CC	AW37	12
		GND	38	HB17_N_CC	AW38	12
		*7 VIO_B_M2C	39	GND		
		GND	40	*7 VIO_B_M2C		

***1 RES1,0**

It is connected to test point.

***2 SCL,SDA**

Test point for I2C communication with the FMC mezzanine card

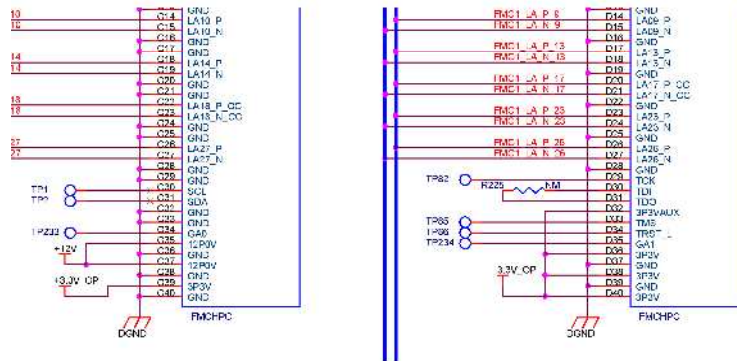


Figure8-5 SDA,SCL,GA1/0 FMC1-JTAG Circuit Structure

***3 GA[1:0]**

It is connected to test point.

***4 FMC1 – JTAG(TCK,TMS,TDI,TDO,TRST_L)**

TDI and TDO have a loopback structure for JTAG communication from the FMC mezzanine card. (TCK, TMS and TRST_L are used for test point only)

By default, this loopback function is not provided because the R225 resistor is not installed.

***5 PG_C2M,PG_M2C**

It is connected to the test point and the pull-up resistor to the 3.3V power supply.



Figure8-6 PG_C2M,PG_M2C Circuit Structure

***6 PRSNT_M2C**

It is connected to the FPGA and the pull-up resistor to the 2.5V power supply.

*7 Power Supply

The board provides a 12V to the 12P0V pin and a 3.3V to the 3P3V and 3P3VAUX pins. 5V, 3.3V and 2.5V are also selectable for VADJ pins as shown in Figure 8-8. The target pins are E39, F40, G39 and H40. The voltage supply can be provided by short-circuiting one portion of JP3 and JP4 respectively. The power status can be monitored by the adjacent LED.

Caution:

Do not short-circuit more than two portions of JP3 and JP4 respectively.
Short-circuit the same portion of JP3 and JP4.

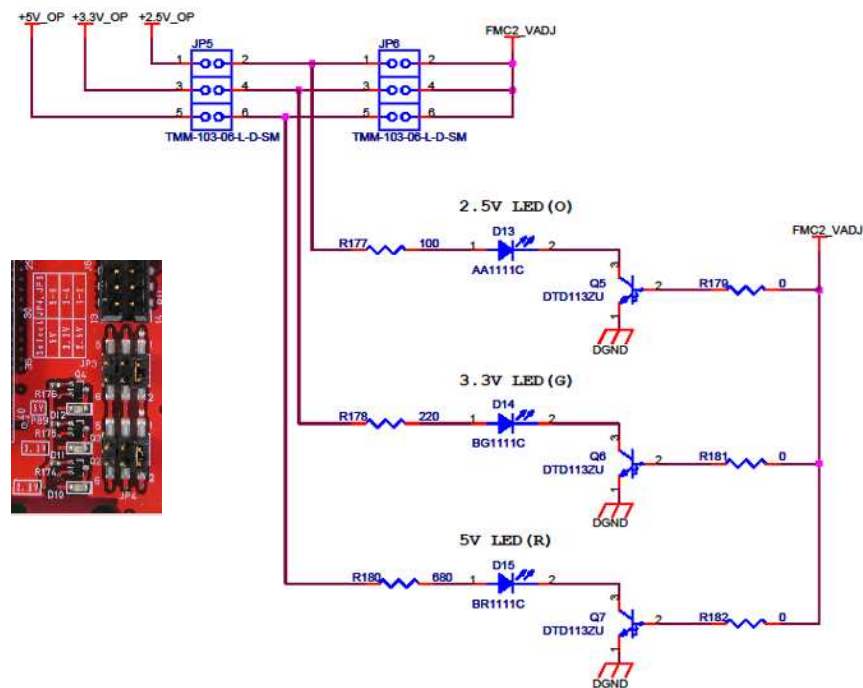


Figure8-7 VADJ Circuit Structure

* VIO_B_M2C

The VIO_B_M2C terminal of the J39 and K40 pins can be monitored by TP95.

* VREF_A_M2C, VREF_B_M2C

The board provides the TP90 Test Pad to monitor the VREF_A_M2C terminal of the H1 pin and the TP92 Test Pad to monitor the VREF_B_M2C terminal of the K1 pin.

8.3.2. FMC2 HPC Connector (High-Pin Count)

The board uses the High-Pin Count connector. Due to limitation of the number of FPGA pins (Banks), all FMC connector pins are not connected. The connector is interfaced as shown below.

HighSpeed: XC6VLX240T/365T TX 8ch RX 8ch
 XC6VLX550T/XC6VSX475T TX 10ch RX 10ch
 LowSpeed: XC6VLX240T/365T LA 34Pair (72) HA 24Pair (48)
 XC6VLX550T/XC6VSX475T LA 34Pair (72) HA 24Pair (48) HB 20Pair (40)

Table 3 shows the FMC2 connector pinout table for FPGA.

Table 3 FMC2 Connector Pinout Table

Bank No.	Pin No.	A		B	PinNo.	Bank No.
		GND	1	*1 RES1		
MGTRXP2_117	F7	DP1_M2C_P	2	GND		
MGTRXN2_117	F8	DP1_M2C_N	3	GND		
		GND	4	DP9_M2C_P	AP7	MGTRXP3_111
		GND	5	DP9_M2C_N	AP8	MGTRXN3_111
MGTRXP1_117	G5	DP2_M2C_P	6	GND		
MGTRXN1_117	G6	DP2_M2C_N	7	GND		
		GND	8	DP8_M2C_P	AR5	MGTRXP2_111
		GND	9	DP8_M2C_N	AR6	MGTRXN2_111
MGTRXP0_117	H7	DP3_M2C_P	10	GND		
MGTRXN0_117	H8	DP3_M2C_N	11	GND		
		GND	12	DP7_M2C_P	J5	MGTRXP3_116
		GND	13	DP7_M2C_N	J6	MGTRXN3_116
MGTRXP2_116	L5	DP4_M2C_P	14	GND		
MGTRXN2_116	L6	DP4_M2C_N	15	GND		
		GND	16	DP6_M2C_P	N5	MGTRXP1_116
		GND	17	DP6_M2C_N	N6	MGTRXN1_116
MGTRXP0_116	P7	DP5_M2C_P	18	GND		
MGTRXN0_116	P8	DP5_M2C_N	19	GND		
		GND	20	GBTCLK1_M2C_P	M8	MGTREFCLK0P_116
		GND	21	GBTCLK1_M2C_N	M7	MGTREFCLK0N_116
MGTTXP2_117	G1	DP1_C2M_P	22	GND		
MGTTXN2_117	G2	DP1_C2M_N	23	GND		
		GND	24	DP9_C2M_P	AR1	MGTTXP3_111
		GND	25	DP9_C2M_N	AR2	MGTTXN3_111
MGTTXP1_117	H3	DP2_C2M_P	26	GND		
MGTTXN1_117	H4	DP2_C2M_N	27	GND		
		GND	28	DP8_C2M_P	AT3	MGTTXP2_111
		GND	29	DP8_C2M_N	AT4	MGTTXN2_111
MGTTXP0_117	J1	DP3_C2M_P	30	GND		
MGTTXN0_117	J2	DP3_C2M_N	31	GND		
		GND	32	DP7_C2M_P	K3	MGTTXP3_116
		GND	33	DP7_C2M_N	K4	MGTTXN3_116
MGTTXP2_116	L1	DP4_C2M_P	34	GND		
MGTTXN2_116	L2	DP4_C2M_N	35	GND		
		GND	36	DP6_C2M_P	M3	MGTTXP1_116
		GND	37	DP6_C2M_N	M4	MGTTXN1_116
MGTTXP0_116	N1	DP5_C2M_P	38	GND		
MGTTXN0_116	N2	DP5_C2M_N	39	GND		
		GND	40	*1 RES0		

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	*5 PG_C2M		
MGTTXP3_117	F3	DP0_C2M_P	2	GND		
MGTTXN3_117	F4	DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P	G10	MGTREFCLK0P_117
		GND	5	GBTCLK0_M2C_N	G9	MGTREFCLK0N_117
MGTRXP3_117	E5	DP0_M2C_P	6	GND		
MGTRXN3_117	E6	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	N40	17
		GND	9	LA01_N_CC	N41	17
17	N38	LA06_P	10	GND		
17	N39	LA06_N	11	LA05_P	L41	17
		GND	12	LA05_N	L42	17
		GND	13	GND		
17	P40	LA10_P	14	LA09_P	N35	17
17	P41	LA10_N	15	LA09_N	N34	17
		GND	16	GND		
		GND	17	LA13_P	P42	17
17	T34	LA14_P	18	LA13_N	R42	17
17	T35	LA14_N	19	GND		
		GND	20	LA17_P_CC	AA35	16
		GND	21	LA17_N_CC	Y35	16
16	V40	LA18_P_CC	22	GND		
16	W40	LA18_N_CC	23	LA23_P	W37	16
		GND	24	LA23_N	Y37	16
		GND	25	GND		
16	V38	LA27_P	26	LA26_P	W35	16
16	W38	LA27_N	27	LA26_N	V35	16
		GND	28	GND		
		GND	29	*4 TCK		
		*2 SCL	30	*4 TDI		
		*2 SDA	31	*4 TDO		
		GND	32	3P3VAUX		
		GND	33	*4 TMS		
		*3 GA0	34	*4 TRST_L		
		12P0V	35	*3 GA1		
		GND	36	3P3V		
		12P0V	37	GND		
		GND	38	3P3V		
		3P3V	39	GND		
		GND	40	3P3V		

Bank No.	Pin No.	E		F	PinNo.	Bank No.
		GND	1	*5 PG_M2C		
25	P27	HA01_P_CC	2	GND		
25	R27	HA01_N_CC	3	GND		
		GND	4	HA00_P_CC	K38	25
		GND	5	HA00_N_CC	J38	25
25	J37	HA05_P	6	GND		
25	J36	HA05_N	7	HA04_P	L35	25
		GND	8	HA04_N	L36	25
25	L34	HA09_P	9	GND		
25	M34	HA09_N	10	HA08_P	K33	25
		GND	11	HA08_N	K32	25
25	M31	HA13_P	12	GND		
25	N31	HA13_N	13	HA12_P	N29	25
		GND	14	HA12_N	N30	25
25	R28	HA16_P	15	GND		
25	R29	HA16_N	16	HA15_P	N28	25
		GND	17	HA15_N	P28	25
35	C13	HA20_P	18	GND		
35	D12	HA20_N	19	HA19_P	D13	35
		GND	20	HA19_N	E13	35
21	AT26	HB03_P	21	GND		
21	AU27	HB03_N	22	HB02_P	AM22	21
		GND	23	HB02_N	AL22	21
21	AM24	HB05_P	24	GND		
21	AL24	HB05_N	25	HB04_P	AN24	21
		GND	26	HB04_N	AN25	21
21	AK22	HB09_P	27	GND		
21	AJ22	HB09_N	28	HB08_P	AR24	21
		GND	29	HB08_N	AT24	21
21	AJ23	HB13_P	30	GND		
21	AK23	HB13_N	31	HB12_P	AW25	21
		GND	32	HB12_N	AW26	21
21	AM23	HB19_P	33	GND		
21	AN23	HB19_N	34	HB16_P	AT25	21
		GND	35	HB16_N	AR25	21
		HB21_P	36	GND		
		HB21_N	37	HB20_P		
		GND	38	HB20_N		
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*7 VREF_A_M2C		
35	E14	CLK1_M2C_P	2	*6 PRSNT_M2C_L	C15	35
35	F14	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	L12	35
		GND	5	CLK0_M2C_N	M12	35
17	R39	LA00_P_CC	6	GND		
17	P38	LA00_N_CC	7	LA02_P	L39	17
		GND	8	LA02_N	L40	17
17	M38	LA03_P	9	GND		
17	M39	LA03_N	10	LA04_P	M36	17
		GND	11	LA04_N	M37	17
17	M41	LA08_P	12	GND		
17	M42	LA08_N	13	LA07_P	N36	17
		GND	14	LA07_N	P37	17
17	R37	LA12_P	15	GND		
17	T37	LA12_N	16	LA11_P	R35	17
		GND	17	LA11_N	R34	17
17	U36	LA16_P	18	GND		
17	T36	LA16_N	19	LA15_P	R40	17
		GND	20	LA15_N	T40	17
16	U32	LA20_P	21	GND		
16	U33	LA20_N	22	LA19_P	W36	16
		GND	23	LA19_N	V36	16
16	AA34	LA22_P	24	GND		
16	Y34	LA22_N	25	LA21_P	V33	16
		GND	26	LA21_N	W33	16
16	U39	LA25_P	27	GND		
16	V39	LA25_N	28	LA24_P	Y40	16
		GND	29	LA24_N	Y39	16
16	W42	LA29_P	30	GND		
16	Y42	LA29_N	31	LA28_P	AA36	16
		GND	32	LA28_N	AA37	16
16	U37	LA31_P	33	GND		
16	U38	LA31_N	34	LA30_P	Y38	16
		GND	35	LA30_N	AA39	16
16	V41	LA33_P	36	GND		
16	W41	LA33_N	37	LA32_P	U42	16
		GND	38	LA32_N	U41	16
		VADJ	39	GND		
		GND	40	VADJ		

Bank No.	Pin No.	J		K	PinNo.	Bank No.
		GND	1	*7 VREF_B_M2C		
17	P36	CLK3_M2C_P	2	GND		
17	P35	CLK3_M2C_N	3	GND		
		GND	4	CLK2_M2C_P	V34	16
		GND	5	CLK2_M2C_N	U34	16
25	H39	HA03_P	6	GND		
25	H38	HA03_N	7	HA02_P	J40	25
		GND	8	HA02_N	J41	25
25	K35	HA07_P	9	GND		
25	K34	HA07_N	10	HA06_P	K37	25
		GND	11	HA06_N	L37	25
25	H40	HA11_P	12	GND		
25	H41	HA11_N	13	HA10_P	M33	25
		GND	14	HA10_N	M32	25
25	L31	HA14_P	15	GND		
25	L32	HA14_N	16	HA17_P_CC	E15	35
		GND	17	HA17_N_CC	F15	35
35	M13	HA18_P	18	GND		
35	N13	HA18_N	19	HA21_P	B14	35
		GND	20	HA21_N	C14	35
35	J13	HA22_P	21	GND		
35	K13	HA22_N	22	HA23_P	K14	35
		GND	23	HA23_N	L14	35
21	AV26	HB01_P	24	GND		
21	AU26	HB01_N	25	HB00_P_CC	AU23	21
		GND	26	HB00_N_CC	AU24	21
21	AP23	HB07_P	27	GND		
21	AR23	HB07_N	28	HB06_P_CC	AP25	21
		GND	29	HB06_N_CC	AP26	21
21	AV24	HB11_P	30	GND		
21	AV25	HB11_N	31	HB10_P	BA25	21
		GND	32	HB10_N	AY25	21
21	BA26	HB15_P	33	GND		
21	BA27	HB15_N	34	HB14_P	BB26	21
		GND	35	HB14_N	BB27	21
21	AY27	HB18_P	36	GND		
21	AW27	HB18_N	37	HB17_P_CC	AK24	21
		GND	38	HB17_N_CC	AL25	21
		*7 VIO_B_M2C	39	GND		
		GND	40	*7 VIO_B_M2C		

***1 RES1,0**

It is connected to test point.

***2 SCL,SDA**

Test point for I2C communication with the FMC mezzanine card.

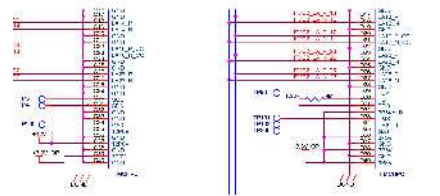


Figure8-8 SDA,SCL,GA1/0 FMC1-JTAG Circuit Structure

***3 GA[1:0]**

It is connected to test point.

***4 FMC2-JTAG (TCK,TMS,TDI,TDO,TRST_L)**

TDI and TDO have a loopback structure for JTAG communication from the FMC mezzanine card.

(TCK and TMS,TRST_L are used for test point only)

By default, this loopback function is not provided because the R227 resistor is not installed.

***5 PG_C2M,PG_M2C**

It is connected to the test point and the pull-up resistor to the 3.3V power supply.

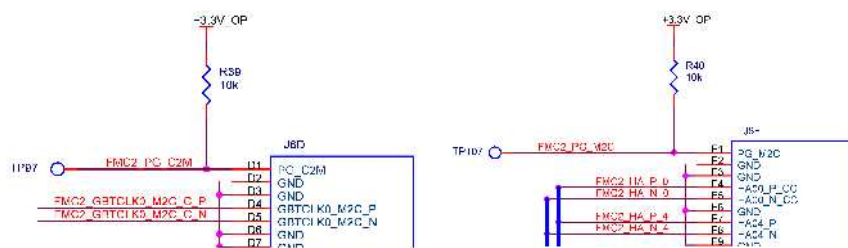


Figure8-9 PG_C2M,PG_M2C Circuit Structure

***6 PRSNT_M2C**

It is connected to the FPGA and the pull-up resistor to the 2.5V power supply.

*7 Power Supply

The board provides a 12V to the 12P0V pin and a 3.3V to the 3P3V and 3P3VAUX pins. 5V, 3.3V and 2.5V are also selectable for VADJ pins as shown in Figure 8-11. Target pins are E39, F40, G39 and H40.

The voltage supply can be provided by short-circuiting one portion of JP5 and JP6 respectively. The power status can be monitored by the adjacent LED.

Caution:

Do not short-circuit more than two portions of JP5 and JP6 respectively.

Short-circuit the same portion of JP5 and JP6.

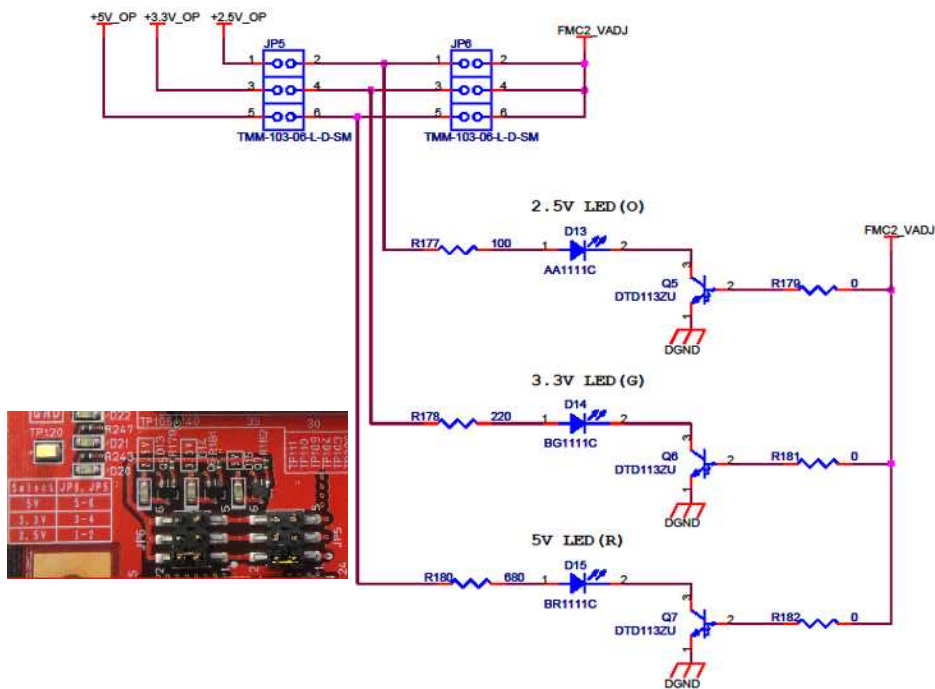


Figure8-10 VADJ Circuit Structure

* VIO_B_M2C

The VIO_B_M2C terminal of the J39 and K40 pins can be monitored by the onboard TP111 test point.

* VREF_A_M2C,VREF_B_M2C

The board provides TP107 test pad to monitor the VREF_A_M2C terminal of the H1 pin and the TP108 test pad to monitor the VREF_B_M2C terminal of the K1 pin.

8.3.3. FMC3 LPC Connector (Low-Pin Count)

The board uses the Low-Pin Count connector. Due to limitation of the number of FPGA pins (Banks), all FMC connector pins are not connected. The connector is interfaced as shown below.

HighSpeed: XC6VLX240T/365T TX 0ch RX 0ch

XC6VLX550T/XC6VVSX475T TX 1ch RX 1ch

LowSpeed: XC6VLX240T/365T LA 0Pair (0)

XC6VLX550T/XC6VVSX475T LA 34Pair (72)

Table 4 shows the FMC3 connector pinout table for FPGA.

Table 4 FMC3 Connector Pinout Table

Bank No.	Pin No.	C		D	Pin No.	Bank No.
		GND	1	*4 PG_C2M		
MGTTXP2_118	C1	DP0_C2M_P	2	GND		
MGTTXN2_118	C2	DP0_C2M_N	3	GND		
		GND	4	GBTCLK0_M2C_P	A10	MGTREFCLK1P_118
		GND	5	GBTCLK0_M2C_N	A9	MGTREFCLK1N_118
MGTRXP2_118	B7	DP0_M2C_P	6	GND		
MGTRXN2_118	B8	DP0_M2C_N	7	GND		
		GND	8	LA01_P_CC	L26	28
		GND	9	LA01_N_CC	L25	28
28	L27	LA06_P	10	GND		
28	K27	LA06_N	11	LA05_P	C31	28
		GND	12	LA05_N	D31	28
		GND	13	GND		
28	C30	LA10_P	14	LA09_P	A29	28
28	D30	LA10_N	15	LA09_N	A30	28
		GND	16	GND		
		GND	17	LA13_P	B29	28
28	N24	LA14_P	18	LA13_N	C29	28
28	N25	LA14_N	19	GND		
		GND	20	LA17_P_CC	J23	38
		GND	21	LA17_N_CC	K23	38
38	N21	LA18_P_CC	22	GND		
38	M21	LA18_N_CC	23	LA23_P	H26	38
		GND	24	LA23_N	H25	38
		GND	25	GND		
38	B27	LA27_P	26	LA26_P	M22	38
38	A27	LA27_N	27	LA26_N	M23	38
		GND	28	GND		
		GND	29	*3 TCK		
		*1 SCL	30	*3 TDI		
		*1 SDA	31	*3 TDO		
		GND	32	3P3VAUX		
		GND	33	*3 TMS		
		*2 GA0	34	*3 TRST_L		
		12P0V	35	*2 GA1		
		GND	36	3P3V		
		12P0V	37	GND		
		GND	38	3P3V		
		3P3V	39	GND		
		GND	40	3P3V		

Bank No.	Pin No.	G		H	Pin No.	Bank No.
		GND	1	*6 VREF_A_M2C		
25	J42	CLK1_M2C_P	2	*5 PRSNT_M2C_L	G28	28
25	K42	CLK1_M2C_N	3	GND		
		GND	4	CLK0_M2C_P	P30	25
		GND	5	CLK0_M2C_N	P31	25
28	R25	LA00_P_CC	6	GND		
28	P25	LA00_N_CC	7	LA02_P	E30	28
		GND	8	LA02_N	F30	28
28	A31	LA03_P	9	GND		
28	B31	LA03_N	10	LA04_P	H28	28
		GND	11	LA04_N	H29	28
28	J28	LA08_P	12	GND		
28	K28	LA08_N	13	LA07_P	M26	28
		GND	14	LA07_N	M27	28
28	R23	LA12_P	15	GND		
28	P23	LA12_N	16	LA11_P	G29	28
		GND	17	LA11_N	F29	28
38	N23	LA16_P	18	GND		
38	M24	LA16_N	19	LA15_P	F27	28
		GND	20	LA15_N	E28	28
38	K25	LA20_P	21	GND		
38	J25	LA20_N	22	LA19_P	C28	38
		GND	23	LA19_N	B28	38
38	E27	LA22_P	24	GND		
38	D27	LA22_N	25	LA21_P	H24	38
		GND	26	LA21_N	G24	38
38	A26	LA25_P	27	GND		
38	A25	LA25_N	28	LA24_P	B26	38
		GND	29	LA24_N	C25	38
38	C26	LA29_P	30	GND		
38	D26	LA29_N	31	LA28_P	D25	38
		GND	32	LA28_N	E25	38
38	F25	LA31_P	33	GND		
38	F24	LA31_N	34	LA30_P	G26	38
		GND	35	LA30_N	F26	38
38	P20	LA33_P	36	GND		
38	N20	LA33_N	37	LA32_P	P21	38
		GND	38	LA32_N	P22	38
		VADJ	39	GND		
		GND	40	VADJ		

***1 SCL,SDA**

Test point for I2C communication with the FMC mezzanine card.

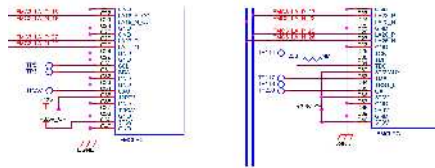


Figure8-11 SDA,SCL,GA1/0 FMC3-JTAG Circuit Structure

***2 GA[1:0]**

It is connected to test point.

***3 FMC3 – JTAG(TCK,TMS,TDI,TDO,TRST_L)**

TDI and TDO have a loopback structure for JTAG communication from the FMC mezzanine card.

(TCK, TMS and TRST_L are used for test point only)

By default, this loopback function is not provided because the R230 resistor is not installed.

***4 PG_C2M**

This is connected to the test point and a pull-up resistor to the 3.3V power supply.

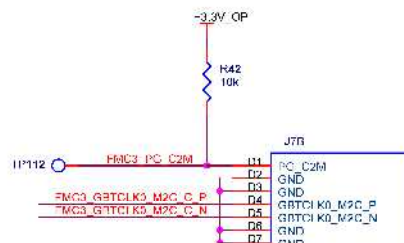


Figure8-12 PG_C2M Circuit Structure

***5 PRSNT_M2C**

This is connected to the FPGA and a pull-up resistor to the 2.5V power supply.

*6 Power Supply

The board provides a 12V to the 12P0V pin and a 3.3V to the 3P3V and 3P3VAUX pins. 5V, 3.3V and 2.5V are also selectable for VADJ pins as shown in Figure 8-14. Target pins are G39 and H40. The power supply can be provided by short-circuiting one portion of JP7 and JP8 respectively. The power status can be monitored by the adjacent LED.

Caution:

Do not short-circuit more than two portions of JP7 and JP8 respectively.
Short-circuit the same portion of JP7 and JP8.

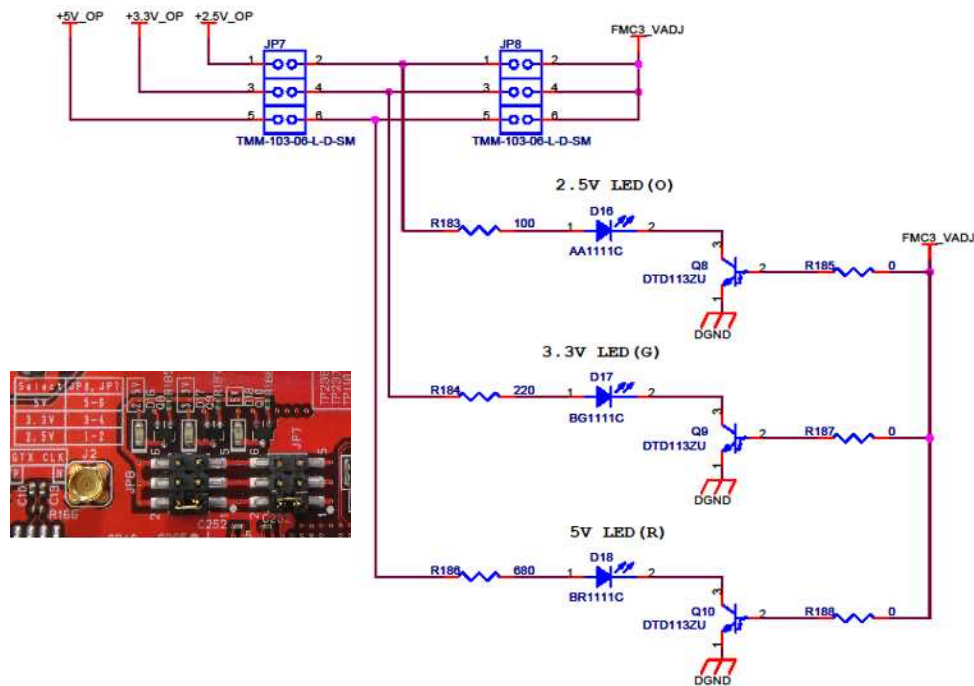


Figure8-13 VADJ Circuit Structure

* VREF_A_M2C

The VREF_A_M2C terminal of the H1 pin can be monitored by the onboard TP113 test pad.

8.4. DDR3 SO-DIMM Interface

The board provides two SanMax 1GByteDDR3 SO-DIMM(SMD-N1G88-13H) connectors.

Tables 5 and 6 show the pinout for FPGA.

Table 5 DDR3 SO-DIMM-1 Pinout Table

Bank No.	Pin No.	Signal Name	Pin No.		Signal Name	Pin No.	Bank No.
	-	VREFDQ	1	2	Vss	-	
	-	Vss	3	4	DQ4	B38	26
26	H36	DQ0	5	6	DQ5	A39	26
26	G36	DQ1	7	8	Vss	-	
	-	Vss	9	10	DQS0#	H35	26
26	C39	DM0	11	12	DQS0	J35	26
	-	Vss	13	14	Vss	-	
26	B37	DQ2	15	16	DQ6	F37	26
26	A37	DQ3	17	18	DQ7	B39	26
	-	Vss	19	20	Vss	-	
26	D38	DQ8	21	22	DQ12	H34	26
26	C38	DQ9	23	24	DQ13	F36	26
	-	Vss	25	26	Vss	-	
26	A41	DQS1#	27	28	DM1	C41	26
26	A40	DQS1	29	30	RESET#	B36	27
	-	Vss	31	32	Vss	-	
26	E38	DQ10	33	34	DQ14	B42	26
26	G34	DQ11	35	36	DQ15	C40	26
	-	Vss	37	38	Vss	-	
26	G37	DQ16	39	40	DQ20	F41	26
26	D42	DQ17	41	42	DQ21	G41	26
	-	Vss	43	44	Vss	-	
26	E40	DQS2#	45	46	DM2	F42	26
26	D40	DQS2	47	48	Vss	-	
	-	Vss	49	50	DQ22	G42	26
26	D41	DQ18	51	52	DQ23	E42	26
26	F40	DQ19	53	54	Vss	-	
	-	Vss	55	56	DQ28	C24	37
37	G23	DQ24	57	58	DQ29	C23	37
37	H23	DQ25	59	60	Vss	-	
	-	Vss	61	62	DQS3#	F22	37
37	B22	DM3	63	64	DQS3	G22	37
	-	Vss	65	66	Vss	-	
37	B24	DQ26	67	68	DQ30	F21	37
37	A24	DQ27	69	70	DQ31	B23	37
	-	Vss	71	72	Vss	-	
27	C36	CKE0	73	74	CKE1(NC)	D36	27
	-	VDD	75	76	VDD	-	

	-	NC	77	78	NC(A15)	D37	27
27	L30	BA2	79	80	A14(NC)	E32	27
	-	VDD	81	82	VDD	-	
27	A32	A12	83	84	A11	B32	27
27	F31	A9	85	86	A7	C33	27
	-	VDD	87	88	VDD	-	
27	B33	A8	89	90	A6	E35	27
27	A34	A5	91	92	A4	A35	27
	-	VDD	93	94	VDD	-	
27	H31	A3	95	96	A2	G31	27
27	B34	A1	97	98	A0	C34	27
	-	VDD	99	100	VDD	-	
27	G33	CK0	101	102	CK1	E34	27
27	G32	CK0#	103	104	CK1#	F34	27
	-	VDD	105	106	VDD	-	
27	F32	A10	107	108	BA1	M28	27
27	M29	BA0	109	110	RAS#	D33	27
	-	VDD	111	112	VDD	-	
27	A36	WE#	113	114	CS0#	J32	27
27	E33	CAS#	115	116	ODT0	C35	27
	-	VDD	117	118	VDD	-	
27	D32	A13	119	120	ODT1(NC)	K29	27
27	K30	CS1#(NC)	121	122	NC	-	
	-	VDD	123	124	VDD	-	
	-	NC	125	126	VREFCA	-	
	-	Vss	127	128	Vss	-	
37	H21	DQ32	129	130	DQ36	K22	37
37	J21	DQ33	131	132	DQ37	D22	37
	-	Vss	133	134	Vss	-	
37	E23	DQS4#	135	136	DM4	A22	37
37	E24	DQS4	137	138	Vss	-	
	-	Vss	139	140	DQ38	E20	37
37	G21	DQ34	141	142	DQ39	F20	37
37	L21	DQ35	143	144	Vss	-	
	-	Vss	145	146	DQ44	C21	37
37	A21	DQ40	147	148	DQ45	D21	37
37	J20	DQ41	149	150	Vss	-	
	-	Vss	151	152	DQS5#	L20	37
37	C20	DM5	153	154	DQS5	K20	37
	-	Vss	155	156	Vss	-	
37	B21	DQ42	157	158	DQ46	K19	37
37	A20	DQ43	159	160	DQ47	L19	37
	-	Vss	161	162	Vss	-	
36	K18	DQ48	163	164	DQ52	G19	36

36	J18	DQ49	165	166	DQ53	F19	36
	-	Vss	167	168	Vss	-	
36	F16	DQS6#	169	170	DM6	E18	36
36	G16	DQS6	171	172	Vss	-	
	-	Vss	173	174	DQ54	J16	36
36	H18	DQ50	175	176	DQ55	E19	36
36	G18	DQ51	177	178	Vss	-	
	-	Vss	179	180	DQ60	P17	36
36	K17	DQ56	181	182	DQ61	P16	36
36	J17	DQ57	183	184	Vss	-	
	-	Vss	185	186	DQS7#	B19	36
36	C18	DM7	187	188	DQS7	C19	36
	-	Vss	189	190	Vss	-	
36	N18	DQ58	191	192	DQ62	G17	36
36	P18	DQ59	193	194	DQ63	D18	36
	-	Vss	195	196	Vss	-	
	-	SA0	197	198	EVENT#	-	
	-	VDDSPD	199	200	SDA	J15	36
	-	SA1	201	202	SCL	B18	36
	-	VTT	203	204	VTT	-	

Table 6 DDR3 SO-DIMM-2 Pinout Table

Bank No.	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Bank No.
	-	VREFDQ	1	2	Vss	-
	-	Vss	3	4	DQ4	AM33
23	AP30	DQ0	5	6	DQ5	AM32
23	AN30	DQ1	7	8	Vss	-
	-	Vss	9	10	DQS0#	AL30
23	AN34	DM0	11	12	DQS0	AL29
	-	Vss	13	14	Vss	-
23	AM31	DQ2	15	16	DQ6	AN29
23	AL31	DQ3	17	18	DQ7	AN33
	-	Vss	19	20	Vss	-
23	AL27	DQ8	21	22	DQ12	AK25
23	AM28	DQ9	23	24	DQ13	AH25
	-	Vss	25	26	Vss	-
23	AN31	DQS1#	27	28	DM1	AR32
23	AP31	DQS1	29	30	RESET#	AU31
	-	Vss	31	32	Vss	-
23	AK29	DQ10	33	34	DQ14	AP33
23	AJ25	DQ11	35	36	DQ15	AP32
	-	Vss	37	38	Vss	-
23	AG28	DQ16	39	40	DQ20	AJ27

23	AR33	DQ17	41	42	DQ21	AJ26	23
	-	Vss	43	44	Vss	-	
23	AU32	DQS2#	45	46	DM2	AW33	23
23	AU33	DQS2	47	48	Vss	-	
	-	Vss	49	50	DQ22	AH26	23
23	AT32	DQ18	51	52	DQ23	AV33	23
23	AK27	DQ19	53	54	Vss	-	
	-	Vss	55	56	DQ28	AT16	33
33	AL15	DQ24	57	58	DQ29	AU17	33
33	AL14	DQ25	59	60	Vss	-	
	-	Vss	61	62	DQS3#	AM14	33
33	AU18	DM3	63	64	DQS3	AN15	33
	-	Vss	65	66	Vss	-	
33	AR17	DQ26	67	68	DQ30	AL17	33
33	AR18	DQ27	69	70	DQ31	AT17	33
	-	Vss	71	72	Vss	-	
22	AV29	CKE0	73	74	CKE1(NC)	BB29	22
	-	VDD	75	76	VDD	-	
	-	NC	77	78	NC(A15)	AW28	22
22	AL26	BA2	79	80	A14(NC)	AW30	22
	-	VDD	81	82	VDD	-	
22	AN26	A12	83	84	A11	AP27	22
22	AV31	A9	85	86	A7	AP28	22
	-	VDD	87	88	VDD	-	
22	AR28	A8	89	90	A6	AY32	22
22	AT29	A5	91	92	A4	AR29	22
	-	VDD	93	94	VDD	-	
22	BA32	A3	95	96	A2	AY33	22
22	AT30	A1	97	98	A0	AR30	22
	-	VDD	99	100	VDD	-	
22	BA30	CK0	101	102	CK1	AU28	22
22	AY30	CK0#	103	104	CK1#	AV28	22
	-	VDD	105	106	VDD	-	
22	AW31	A10	107	108	BA1	AN28	22
22	AM27	BA0	109	110	RAS#	AR27	22
	-	VDD	111	112	VDD	-	
22	AT31	WE#	113	114	CS0#	BB33	22
22	AT27	CAS#	115	116	ODT0	AU29	22
	-	VDD	117	118	VDD	-	
22	AV30	A13	119	120	ODT1(NC)	AY28	22
22	BB31	CS1#(NC)	121	122	NC	-	
	-	VDD	123	124	VDD	-	
	-	NC	125	126	VREFCA	-	
	-	Vss	127	128	Vss	-	

33	AJ17	DQ32	129	130	DQ36	AK14	33
33	AK17	DQ33	131	132	DQ37	AJ15	33
	-	Vss	133	134	Vss	-	
33	AW18	DQS4#	135	136	DM4	AV19	33
33	AY18	DQS4	137	138	Vss	-	
	-	Vss	139	140	DQ38	AR19	33
33	AM16	DQ34	141	142	DQ39	AV18	33
33	AK15	DQ35	143	144	Vss	-	
	-	Vss	145	146	DQ44	AN19	33
33	AM17	DQ40	147	148	DQ45	AK18	33
33	BB18	DQ41	149	150	Vss	-	
	-	Vss	151	152	DQS5#	AY19	33
33	AT19	DM5	153	154	DQS5	BA19	33
	-	Vss	155	156	Vss	-	
33	BB19	DQ42	157	158	DQ46	AJ18	33
33	AN18	DQ43	159	160	DQ47	AU19	33
	-	Vss	161	162	Vss	-	
32	AY24	DQ48	163	164	DQ52	AT20	32
32	BA24	DQ49	165	166	DQ53	AR20	32
	-	Vss	167	168	Vss	-	
32	AU22	DQS6#	169	170	DM6	AL21	32
32	AV23	DQS6	171	172	Vss	-	
	-	Vss	173	174	DQ54	AW23	32
32	AL19	DQ50	175	176	DQ55	AL20	32
32	AM19	DQ51	177	178	Vss	-	
	-	Vss	179	180	DQ60	AK19	32
32	BB24	DQ56	181	182	DQ61	AN21	32
32	BB23	DQ57	183	184	Vss	-	
	-	Vss	185	186	DQS7#	AP20	32
32	BA22	DM7	187	188	DQS7	AN20	32
	-	Vss	189	190	Vss	-	
32	BA20	DQ58	191	192	DQ62	AV20	32
32	AJ20	DQ59	193	194	DQ63	AW20	32
	-	Vss	195	196	Vss	-	
	-	SA0	197	198	EVENT#	-	
	-	VDDSPD	199	200	SDA	AU21	32
	-	SA1	201	202	SCL	AT21	32
	-	VTT	203	204	VTT	-	

8.5. PCI Express Edge Interface

The board allows a PCI Express x8 (8-Lane) Gen2 connection.

Table 7 PCI Express Edge Pinout Table

Bank No.	Pin No.	A		B	Pin No.	Bank No.
	*1	PRSNT1_B	1	+V12	-	
	-	+V12	2	+V12	-	
	-	+V12	3	+V12	-	
		GND	4	GND		
	-	JTAG_TCK	5	SMCLK	-	
	-	JTAG_TDI	6	SMDAT	-	
	-	JTAG_TDO	7	GND		
	-	JTAG_TMS	8	+3.3V	-	
	-	+3.3V	9	JTAG_TRST#	-	
	-	+3.3V	10	+3.3VAUX	-	
BANK 24	W31	PERST#	11	WAKE#	V31	BANK 24
		GND	12	RESERVED	-	
Refer to CLK	U1.6	REFCLK+	13	GND		
	U1.7	REFCLK-	14	PETP0	AD3	MGTRXP3_113
		GND	15	PETN0	AD4	MGTRXN3_113
MGTTXP3_113	AG1	PERP0	16	GND		
MGTTXN3_113	AG2	PERN0	17	PRSNT2#	*1	
		GND	18	GND		
	-	RESERVED	19	PETP1	AE5	MGTRXP2_113
		GND	20	PETN1	AE6	MGTRXN2_113
MGTTXP2_113	AH3	PERP1	21	GND		
MGTTXN2_113	AH4	PERN1	22	GND		
		GND	23	PETP2	AF3	MGTRXP1_113
		GND	24	PETN2	AF4	MGTRXN1_113
MGTTXP1_113	AJ1	PERP2	25	GND		
MGTTXN1_113	AJ2	PERN2	26	GND		
		GND	27	PETP3	AG5	MGTRXP0_113
		GND	28	PETN3	AG6	MGTRXN0_113
MGTTXP0_113	AK3	PERP3	29	GND		
MGTTXN0_113	AK4	PERN3	30	RESERVED	-	
		GND	31	PRSNT2#	*1	
	-	RESERVED	32	GND		
	-	RESERVED	33	PETP4	AJ5	MGTRXP3_112
		GND	34	PETN4	AJ6	MGTRXN3_112
MGTTXP3_112	AL1	PERP4	35	GND		
MGTTXN3_112	AL2	PERN4	36	GND		
		GND	37	PETP5	AL5	MGTRXP2_112
		GND	38	PETN5	AL6	MGTRXN2_112

MGTTXP2_112	AM3	PERP5	39	GND		
MGTTXN2_112	AM4	PERN5	40	GND		
		GND	41	PETP6	AM7	MGTRXP1_112
		GND	42	PETN6	AM8	MGTRXN1_112
MGTTXP1_112	AN1	PERP6	43	GND		
MGTTXN1_112	AN2	PERN6	44	GND		
		GND	45	PETP7	AN5	MGTRXP0_112
		GND	46	PETN7	AN6	MGTRXN0_112
MGTTXP0_112	AP3	PERP7	47	GND		
MGTTXN0_112	AP4	PERN7	48	PRSNT2#	*1	
		GND	49	GND		

*1 The PCI Express lane width depends on the type of a resistor to be installed.

Table 8 shows PCI Express lane width configuration.

Table 8 PCI Express Lane Width Configuration

Device	Lane	
R89	x1	
R90	x4	
R91	x8	Default

8.6. RS232C (UART) Interface

The board provides a RS232C interface as a means of communication with an external device.

RS232C driver IC(U14)TI: MAX3318EI

The RS232C connector (J9) uses 5-pin, 2.54mm pitch pin header.

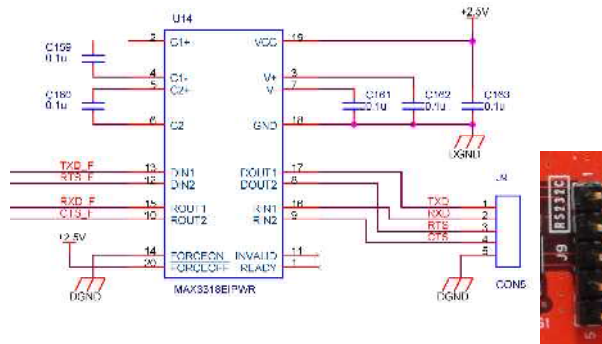


Figure8-14 RS232C Connector Layout

FPGA			MAX3318EIPW		Connector		
Pin No.	Bank	Level	Pin No.	Signal Name	Pin No.	Signal Name	Level
AH29	24	2.5V	13	TXD_F	1	TXD	RS232C
AG29	24		15	RXD_F	2	RXD	
AD30	24		12	RTS_F	3	RTS	
AD31	24		10	CTS_F	4	CTS	
					5	GND	

Table 9 UART Pinout Table

8.7. LED

The board has eight LEDs.

All these LEDs will be turned on when “High” is output from FPGA.



Figure8-15 LED Layout

Table 10 LED Pinout Table

Device		FPGA		
Name	Signal Name	Pin No.	Bank	Level
D1	LED0	AK33	24	2.5V
D2	LED1	SJ32	24	
D3	LED2	Y30	24	
D4	LED3	AA30	24	
D5	LED4	AA31	24	
D6	LED5	AB31	24	
D7	LED6	R32	24	
D8	LED7	T32	24	

8.8. GPIO Interface

The board has a 14 pin header (J15). Of them, 10 signals are connected to FPGA.

The interface has a 2.5V voltage level.

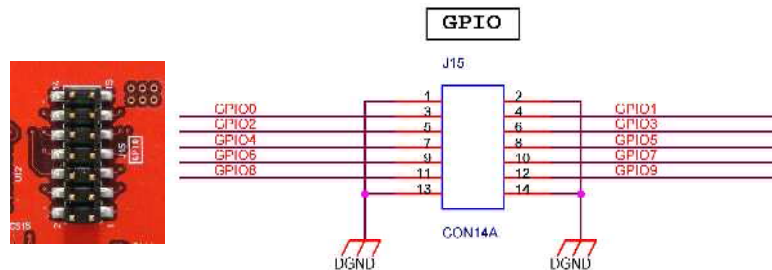


Figure8-16 GPIO Pin Layout

Table 11 GPIO Pinout Table

Bank No.	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Bank No.
	-	GND	1	2	GND	-
13	AL34	GPIO0	3	4	GPIO1	AK34
13	AU39	GPIO2	5	6	GPIO3	A32
15	AB33	GPIO4	7	8	GPIO5	AE37
15	AD37	GPIO6	9	10	GPIO7	AJ37
14	AK37	GPIO8	11	12	GPIO9	T42
	-	GND	13	14	GND	-

8.9. DIPSW

The board has an 8-pole DIPSW. When the DIPSW is set to the ON side, it generates “Low” on the associated FPGA pin.

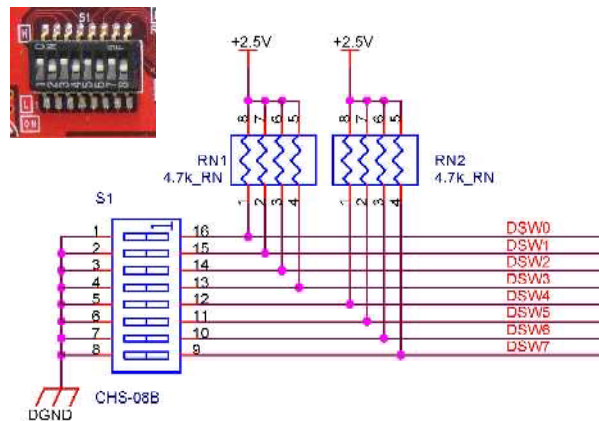


Figure8-17 DIPSW Structure

Table 12 DIPSW Pinout Table

Device		FPGA		
Name	Signal Name	Pin No.	Bank	Level
S1	DSW0	BA16	34	2.5V
	DSW1	BA17	34	
	DSW2	AR14	34	
	DSW3	AT14	34	
	DSW4	BB16	34	
	DSW5	BB17	34	
	DSW6	AP15	34	
	DSW7	AR15	34	

8.10. PUSHSW

The board has four PUSHSWs. When the PUSHSW is held down, it generates “Low” on the associated FPGA pin.

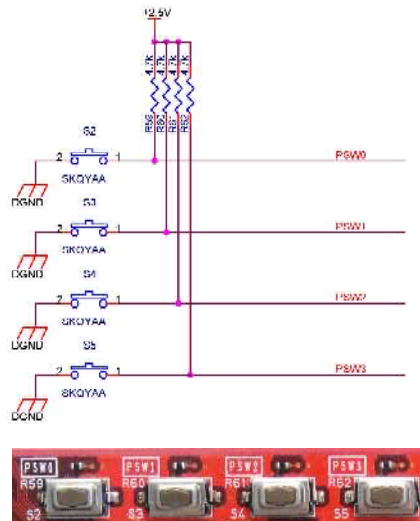


Figure8-18 PUSHSW Structure

Table 13 PUSHSW Pinout

Device		FPGA		
Name	Signal Name	Pin No.	Bank	Level
S2	PSW0	AY17	34	2.5V
S3	PSW1	AW17	34	
S4	PSW2	AT15	34	
S5	PSW3	AU16	34	

8.11. Power Connector for FAN

This is a power supply connector for FAN. It corresponds to the FAN sensor input and is connected to the CONFIG FPGA. When the fan rotation is stopped, the board generates Recon fig. The Recon fig function can be enabled by setting the bit 4 of the CONFIG mode switch (SW1) to ON or disabled by setting it to OFF.



Figure8-19 Power Connector for FAN

Table 14 External Power Supply Connector Pinout Table

Type	No.	1pin	2pin	3pin
Power Connector for FAN	J14	GND	12V	Sensor

8.12. Battery Control

The board has a battery control connector (J13). It is not installed by default.

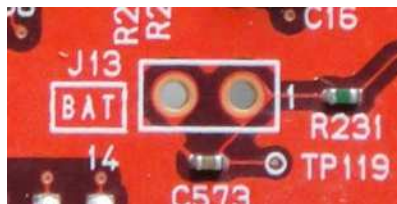


Figure8-20 Battery

Table 15 Battery Control signal Pinout Table

Type	No.	1pin	2pin
Battery Input Connector	J13	+ (1.0 - 2.5V)	- (GND)

8.13. SPI Flash

The board has a 128Mbit SPI Flash memory. All signals are connected to FPGA via level shifter (U13)

Table 16 SPI Flash Pinout Table

SPI Flash		FPGA		
Name	Signal Name	Pin No.	Bank	Level
U12	Serial Data Output(Q)	AC31	24	2.5V
U12	Serial Data Input(D)	AC30	24	
U12	Serial Clcok(C)	AJ31	24	
U12	Chip Select(S)	AK30	24	

9. Configuration

The board allows configuration using microSDCard and NandFlash.

Please see “uSD_CONF_UserManual_V6PCIEX_1_02e.pdf” for more detail of microSDCard configuration.



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